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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 27

Application Number: 09/262,458
Filing Date: March 04, 1999
Appellant(s): POSSLEY, BRIAN D.

Gregory D. Caldwell
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 26, 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existance of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

The amendments after final rejection filed on May 11, 2001 and July 16, 2001 has been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-11, 21-26, and 44 stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

4,611,236	Sato	9-1986
5,780,883	Tran et al	7-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-11 and 21-26 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al in view of Sato.

Tran discloses in figures 3A, 3B, 7, and 8 an integrated circuit comprising a gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions (for example, 148 and 152) and P-type diffusion regions (for example, 146 and 150), the diffusion regions having partially overlying polysilicon gate (54) to form N-type and P-type transistors in which rows of small diffusion regions (146 and 148) are followed by rows of regular-sized diffusion regions (150 and 152) to form two distinct transistor sizes. Sato discloses in figure 9 that one gate can be formed on both N-type and P-type transistors to form the basic cells. Therefore, it would have been obvious to one of ordinary skill in the art to form a single polysilicon gate in Tran on both N-type and P-type transistors to form a basic cell as taught by Sato.

In re claim 21, Tran discloses that the gate array architecture can be used "in the implementation of memories and dynamic logic". Note lines 6 and 7, column 2 of Tran et al. Therefore, it would have been obvious to one of ordinary skill in the art that Tran discloses the "storage medium having instructions stored thereon, said instructions,

when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication" as claimed in claim 21.

Since the scope of the independent claims 1 and 21 was changed by the amendment after final filed on May 11, 2001, a new ground of rejection is also applicable.

Claims 1-11, 21-26 and 44 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Sato.

Sato discloses in figures 7-9 an integrated circuit comprising a gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions (21, 22, and 23) and P-type diffusion regions (11, 12, and 13), the diffusion regions having partially overlying gate (3G) to form N-type and P-type transistors in which rows of small diffusion regions (BC11) are followed by rows of regular-sized diffusion regions (BCL1) to form two distinct transistor sizes. Sato discloses on line 63 of column 1 that 3G are polysilicon gate electrodes. Therefore, it would have been obvious that Sato discloses a single gate electrode formed on two smaller N-type and P-type diffusions to form smaller N- and P- type transistors and another single gate electrode formed on two larger N-type and P-type diffusions to form larger N- and P-type transistors.

In re claim 21, Sato discloses the basic cells being "interconnected by the use of masks having wiring patterns necessary for realizing a functional circuit to meet each customer's specific requirements". Note lines 16-18, column 1 of Sato. Therefore, it would have been obvious to one of ordinary skill in the art that the basic cells in Sato

can form "a storage medium having instructions stored thereon, said instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication" as claimed in claim 21.

(11) Response to Argument

In response to Appellant's arguments in page 12 that "any given diffusion region of FIG. 8 of Tran forms either N-type transistors or P- type transistors, but not both types transistors for a single diffusion region", the Examiner point out that this statement is incorrect. Figures 1 of Appellant's invention shows either N-type transistors or P-type transistors in separate diffusion regions (N-type region or P-type region). There is no teaching that these two type transistors are formed in a single diffusion region as argued by Appellant.

In response to Appellant's arguments in page 12 that "Tran would require additional layers of metallization to connect N-type and P-type transistors", Sato teaches that the basic cells "which are formed in a semiconductor chip in advance, are interconnected by the use of masks having wiring patterns necessary for realizing a functional circuit to meet each customer's specific requirement. Since the gate electrodes are formed in advance over the N-type and P-type transistors as showed in figure 9, there is no need to form additional layers of metallization to connect N-type and P-type transistors as argued.

In response to Appellant's arguments in page 13 that "the combination still fails to provide diffusion regions having partially overlying polysilicon landing where at least one of the regions forms both N-type and P-type transistors", the claims do not have the

features upon which Appellant relies. "one" in claim 1 and 21 refers to "polysilicon gate", not "one of the regions forms both N-type and P-type transistors". As pointed out earlier, figure 1 and the specification does not support for one single diffusion forming both N-type and P-type transistors. Note figure 1 that N-type and P-type diffusions are formed separated from each other. How can a single N-type diffusion region form both N-type and P-type transistor? How can a single P-type diffusion region form both N-type and P-type transistor?

In response to Appellant's arguments in page 14 that the combination of Tran and Sato "show polysilicon landings overlying either N-type diffusion regions or P-type diffusion regions, not overlying at least one diffusion region where both N-type and P-type transistors are formed", Appellant's invention in figure 1 does not show a single diffusion region where both N-type and P-type transistors are formed. The N-type transistors are formed in the N-type diffusion regions and the P-type transistors are formed in the P-type diffusion regions. Where is the single region (N and P) that has N-type and P-type?

In response to Appellant's arguments in page 15 that Tran is directed to gate array architecture for a multiplexer circuit and Sato is directed to a gate array architecture for a RAM cell, Sato clearly discloses on lines 15-19 of column 1 that gate array architecture can form any functional circuit to meet each customer's specific requirement. The teaching in Tran is not limited to a multiplexer circuit and the teaching in Sato is not limited to a RAM cell.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ngan Ngo
Primary Examiner
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Ngan Van Ngo
Primary Examiner

Ngan Ngo
May 6, 2002

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